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TAKE A LOOK INSIDE
Industry Briefs
—see page 7

KEY DATES
For a list of meetings
—see page 8

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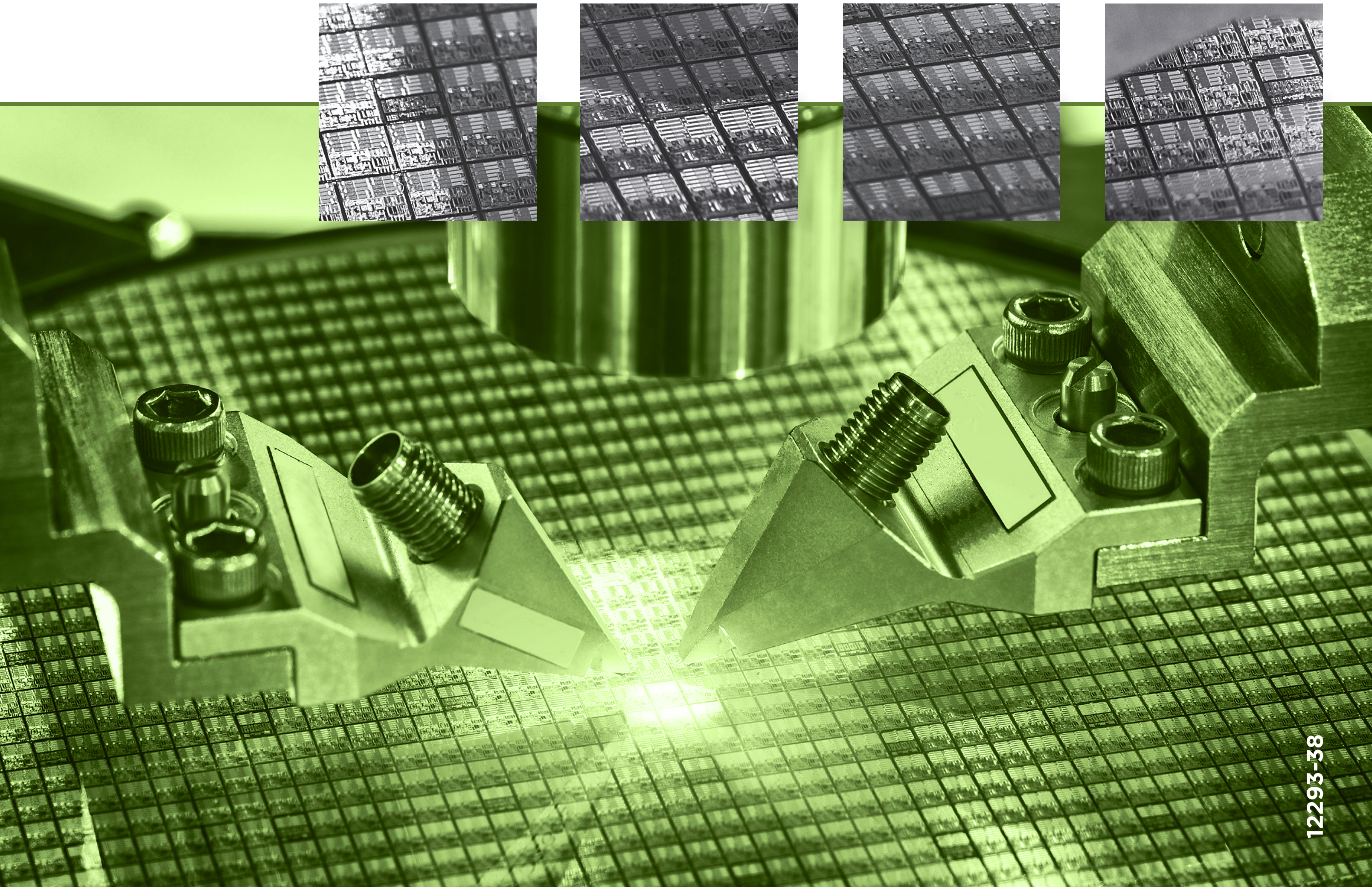
BACUS, SPIE, and community service



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EDITORIAL

BACUS, SPIE, and community service

Ray Shi, *KLA Corporation*

My family lives in a non-single-family community where several homes share one water heater. Recently, the water heater broke down. Our homeowner association consisting of several volunteering board members stepped in and quickly had it fixed. While thanking them for their service, I am reminded of a question asked by our BACUS president recently: why are you sitting on the BACUS Steering Committee?

For me, in addition to representing the company I am working for, I have a profound sense of gratitude towards BACUS and SPIE. In my twenty-five years in the high-tech industry, nearly twenty of which have been in the semiconductor equipment area, I have benefited significantly from attending various SPIE conferences and reading conference proceedings. Thus, I want to reciprocate by performing volunteer work for the community. I am sure that many of the readers feel the same way.

This ecosystem of learning requires not only "students" but also "teachers" who are willing to share their knowledge and expertise. In the most recent Photomask Technology and EUV Lithography conferences held in Monterey, CA, we unsurprisingly saw heavy participation from research institutions. We also witnessed eager presentations from many leading companies. The best example is perhaps ASML. As usual, they have reported and openly shared progress in NA0.33 and NA0.55 EUV scanners along with many other endeavors they are embarking on. Their presence at these conferences should be commended, since through presenting and publishing, ASML is helping to advance the entire community and lithography industry. This in turn benefits everyone, including ASML.

One name conspicuously missing from the conference presenters is a company with a dominant position in the foundry. It is able to crank out chips with the most advanced nodes. Its mask shops are churning out the highest number of leading-edge production masks, and it possibly buys the highest number of advanced equipment from numerous suppliers. There is no denying that this company has benefited from all the open literature published by SPIE. Nonetheless, it is time for the company to reciprocate and participate in these conferences. I am confident that there are plenty of topics that can be shared with the community without sacrificing intellectual properties and most importantly company's bottom lines.

As I am wrapping up this article on a rainy day in wintry California, my family is complaining that it now takes several minutes after turning on the shower head for the hot water to appear with the new water heater. I emailed this observation to our homeowner association president who quickly replied back that he had noticed it and would have it repaired as soon as possible. The spirits of community service are alive and well even in gloomy weather. To paraphrase a famous US president's inauguration speech, I am challenging all the industry players to "ask not (only) what SPIE can do for you, ask (also) what you can do for SPIE."

The opinions expressed in this editorial are personal only and do not constitute those of the company the author is working for.

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Managing Editor/Graphics
Linda DeLano, *SPIE*

Exhibition and Sponsorship Coordinator:
Melissa Valum, *SPIE Sales Representative, Exhibitions and Sponsorships*

BACUS Technical Group Manager
Tim Lamkins, *SPIE*

SPIE.
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
SPIE.org
help@spie.org

Multibeam mask requirements for advanced EUV patterning

M. Chandramouli, B. Liu, Z. Alberti, F. Abboud, *Intel Corporation, MS SC2-12 2200 Mission College Blvd, Santa Clara, CA 95054;* **G. Hochleitner, W. Wroczewski, S. Kuhn, C. Klein, E. Platzgummer,** *IMS Nanofabrication GmbH, Wolfholzgasse 20-24, 2345 Brunn am Gebirge, Austria*

ABSTRACT

Multibeam mask writers (MBMW) from IMS Nanofabrication developed in the last decade are currently being used for leading-edge mask patterning. The ability to utilize low sensitivity resists required to pattern complex mask patterns with good edge placement control made MBMW the tool of choice for leading-edge extreme ultraviolet (EUV) mask patterning. The next generation of High-NA EUV masks will require smaller features, more complex figures, and a reduction of edge placement errors. These requirements may exceed the capability of the current MBMW tools. Recently IMS announced the next generation of MBMW tools to address this challenge. This paper will explore the effectiveness of the proposed improvements in addressing High-NA EUV mask patterning challenges.

Introduction

Multibeam mask writers from IMS (MBMW) were developed from a prototype stage to production during the last decade. The tools have replaced vector-shaped (VSB) e-beam mask writers for the production of the most critical photomasks needed for wafer production. As outlined in several references, the motivation to develop a new class of writers was the assessment that VSB writers would not be able to meet the mask litho requirements without a significant increase in mask write times.[1,2,3] The current generation of MBMW mask writers has been in production since 2016.[4,5,6,7] They are the tool of choice for printing binary EUV masks. High-NA EUV masks[8,9,10] will require a reduction in minimum feature size (MFS) and a reduction of edge placement errors as illustrated in Figure 1. Additionally, it is expected that curvilinear mask patterning will also be deployed in the near future.[11,12,13] The next section will discuss the ability of the current generation of multibeam writers (MBMW101, MBMW201, MBMW261) to meet these requirements.

Patterning Challenges

High-NA EUV masks will require several improvements in mask capabilities[14,15] over conventional EUV masks. Due to its superior resolution, the minimum feature size required on the mask is projected to reduce to sub-30 nm sizes. In addition, the mask edges placement errors such as critical dimension (CD) control and pattern placement control will need to be improved. For the CD improvements and MFS improvements, the process blur needs to be lowered. Both writer and resist improvements will be needed to realize a smaller process blur. On the resist side, slower, less-sensitive resists will be required to reduce the resist blur.[16] On the writer's side, smaller spot sizes than the current generation 20nm and 16nm options will be needed. Both changes will have to be implemented to reduce the critical dimension (CD) errors, line edge roughness (LER), and line width roughness (LWR) variation. Additional hardware improvements will be needed to improve pattern placement accuracy.

Figure 1 compares the trend in mask requirements with the capability of current generation MBMW261 and older tools. As shown, it is expected that the current tools will not be able to meet the edge placement requirements of future nodes. Additionally, the write time using these tools is expected to significantly increase due to the combination of smaller spots and less sensitive CAR. This scenario of taking too long to print a mask and not meeting all the requirements is analogous to the situation that led the industry to develop multibeam. A newer, evolutionary generation such as the recently announced IMS tool called the MBMW301[17] will address many of the gaps the current generation has.

IMS has outlined several key improvements for the MBMW301 including a smaller spot size (11nm), newer optics, a new source, lower distortion, and an improved datapath. Since the MBMW301 is not expected to come online until 2023, there is a desire to confirm that these changes translate into improved mask patterning capability using an existing 201 class tool.

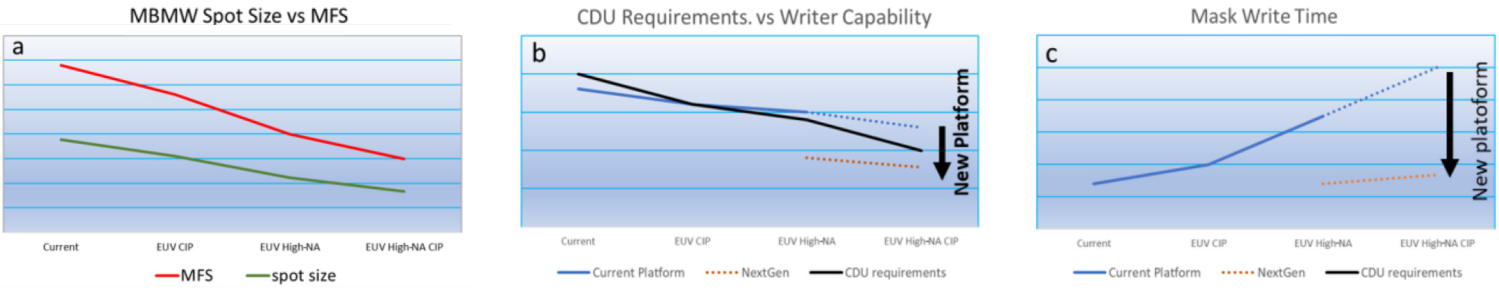


Figure 1. Impact of mask requirement versus mask writer capability highlighting the need for a new platform. (a) MFS trends will require a smaller spot size. (b) CDU requirements are projected to exceed the capability of the current generation MBMW201 and require the new generation MBMW301. (c) Assessment of mask writer time trends showing for future nodes write time will significantly increase unless MBM301 is used.

Experimental

Three key improvement items targeted for the MBMW301 were selected for testing: new write modes, smaller spot sizes, and reduced distortion. Testing was divided into three groups as summarized in the following. Test A examined the impact of write mode changes using a 20nm spot size. Test B evaluated the improvements offered by the reduction of spot size to 10nm. Test C probed the combined effects of smaller spot size (10nm), reduced distortion, and write mode. Test C is the closest to an MBMW301 emulation mode that can be obtained using the MBMW201 tools. Due to the HW differences, the exposure times for many of the tests are longer than the normal reference and longer than what is expected for the MBMW301. It is not expected that this difference will affect the results.

To facilitate the tests, a production MBMW201 was configured with a custom aperture plate system (APS) which is capable of forming a 10nm spot. Custom software was also installed to enable the testing of new write mode options. A mixture of optical and EUV substrates was used. A current generation slow chemically amplified resist (CAR) was used for most of the testing, however new slower resists with reduced blur were also exposed to determine if a better resolution could be obtained using the 10nm spot. Metrology was performed using industry-available CDSEM and registration tools. Internally developed software was used for the LER and LWR assessments. The tests primarily relied on local CD uniformity (LCDU) and local placement as these are the most sensitive to writer performance and are not convolved with global, cross-plate signatures.

Results

The results of the write mode test, Test A are summarized in Figure 2. Two different write mode factors with two levels each were tested. Factor A with levels E and F and Factor B with levels G and H. It is clear from the data that Factor B strongly affects LCDU and local placement performance while Factor A may only have a weak effect at best.

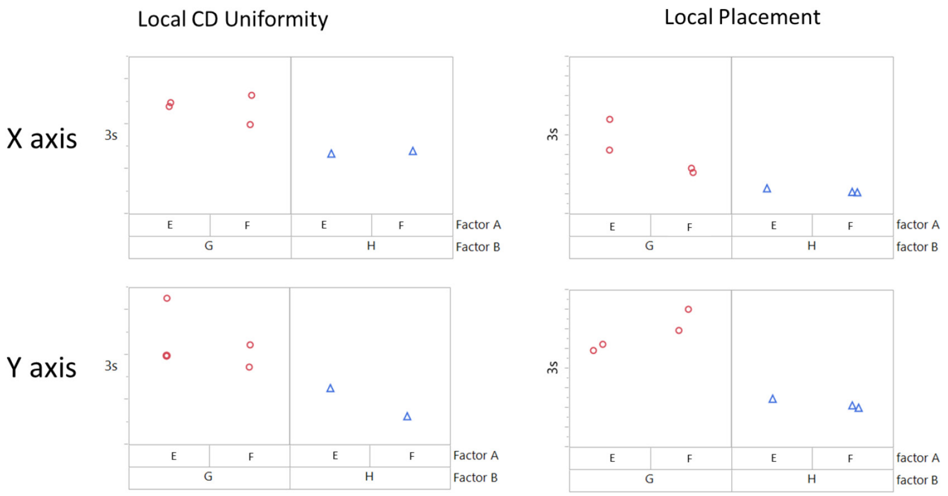


Figure 2. Assessment of write mode impact using 20nm spots (Test A) on LCDU 3 sigma and local placement 3 sigma.

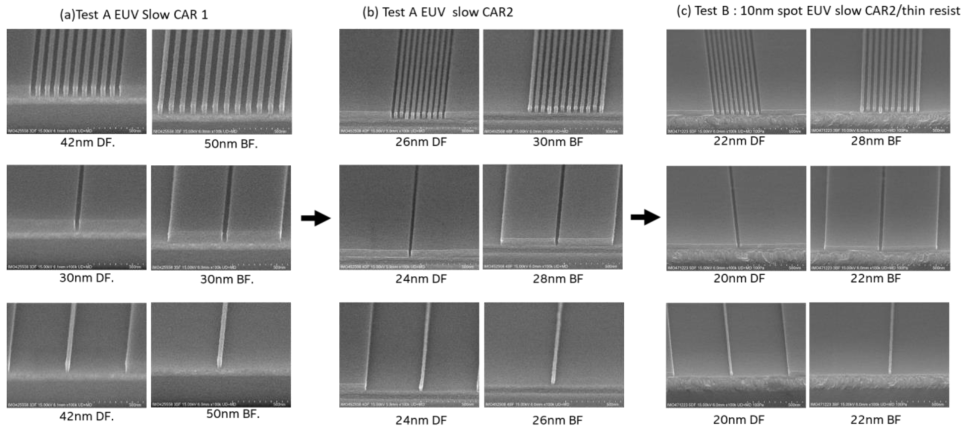


Figure 3. Resolution comparison between (a) slow CAR1 and (b) slow CAR2 resists at the same Test A condition. The improvement in MFS offered by Test B with thinner CAR2 is apparent in (c). Note the 10nm images in (c) also show improved LER over both 20nm cases.

Figure 3 shows a comparison of resist cross sections at different conditions: the current generation slow CAR at 20nm, slower resist CAR2 printed at 20nm, and slower CAR2 printed using the 10 nm spot size. Comparing Figure 3a and 3b, it is clear the 20nm with the slower CAR2 has better resolution. Additionally, as shown in Figure 3b, switching to 10nm beams with the same resist (slightly thinned to avoid pattern collapse) results in further improvements in resolution. These results confirm that a suitable resist is needed along with smaller spot sizes to achieve MFS capability. The MFS with the 10nm spot is in the 20nm range, consistent with projected requirements for High-NA EUV masks. Visually, the 10nm images also show improved LER, another parameter that is expected to be more critical for that application. LER impacts will be further quantified and discussed later in this paper.

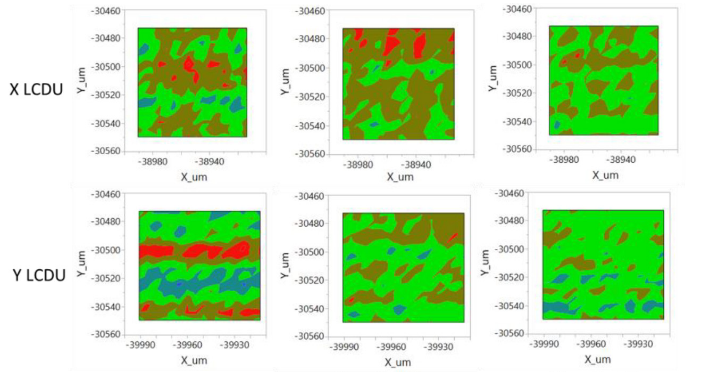
The impact of Tests A, B, and C on LCDU is shown in Figure 4. The LCDU 3 sigma is reduced in tests B and C, however, the additional distortion improvement in test C did not result in additional LCDU improvements. Since the reduction in LCDU 3s is comparable between the two 10nm test conditions, B and C, the spot size reduction is apparently the primary factor in improving LCDU by a factor greater than 1.3. This is consistent with the improvement targets for the High-NA EUV mask process.

An additional test was performed using a long-range stripe CD pattern. Figure 5 summarizes the results of these tests which compare Test A, B, and C versus the current production write mode POR.

Although Test A, B, and C all offer a similar reduction in CDU (1.3x to 1.6x) compared to POR, it is apparent that noise level is significantly reduced in the two 10nm test cases, B and C. The noise reduction allows the detection of an underlying systematic signature. Assuming the root cause of this signature can be eliminated, the estimated CDU for this pattern approaches 0.2nm 3s.

As discussed in the introduction, another important parameter that will need to be improved for High-NA patterning is LER. The improvement in LER and LWR with the different test conditions was checked using the same patterns shown in Figures 4 and 5. The results which are summarized in Figure 6 show significant reductions in LER and LWR in the long-range pattern (a). The improvement of the LER power spectrum for the local CD pattern is shown in figure (b).

The impact of test conditions on local placement is shown in Figure 7. Test B does not show any improvement compared to the POR mode. This is not surprising as the distortion between the two test cases is the same. Only a modest reduction in local registration was obtained as seen in C-g which was printed with a reduced distortion error condition. An additional test using a different write mode, Test C-h, resulted in a major reduction in local reg errors. The errors were observed to be reduced by nearly a factor of 3.



Current Performance Reference (ref)

10nm Test B 3s reduction factor (ref/F) X/Y: 1.5x/1.3x

10nm Test C 3s reduction factor (ref/F) X/Y: 1.7x/1.3x

Figure 4. LCDU comparisons between Test A, B, and C showing LCDU is improved by using the 10nm spot size.

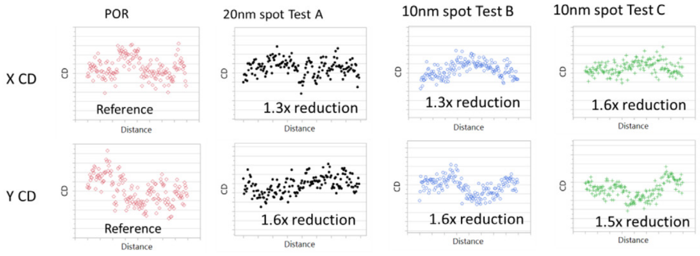


Figure 5. Comparison of CDU measured using a long range stripe pattern. Significant improvement is seen using all three test conditions A, B, and C, however, significant noise reduction is observed in the two 10nm spot size test cases B and C.

One large field layout was exposed using the 10nm test C condition. The write time was 3.7x longer than the write time of the same layout printed at 20nm. The MBMW301 write time is expected to match the current production write time even with a smaller spot and higher dose.

Conclusions

The tests discussed in this paper confirm that improvements targeted for the MBMW301 platform should result in tangible and significant improvements in LCDU, LER, local registration, and resolution. Although an MBMW201 with the test C condition meets many of the lithography requirements for High-NA mask production, the write time in this mode is significantly longer than the current MBMW write time. The MBMW301 is expected to provide improved capability at similar writes times obtained using the 20nm beams with the current generation of tools.

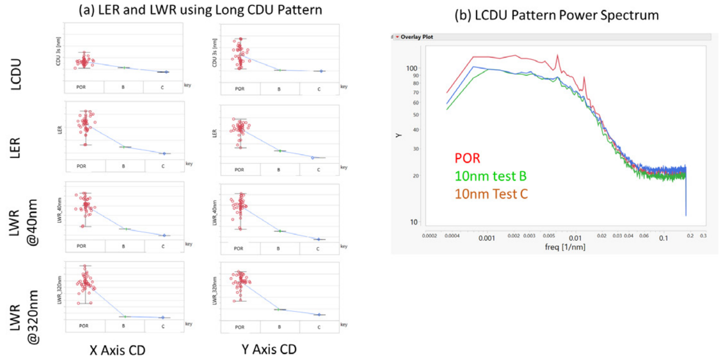
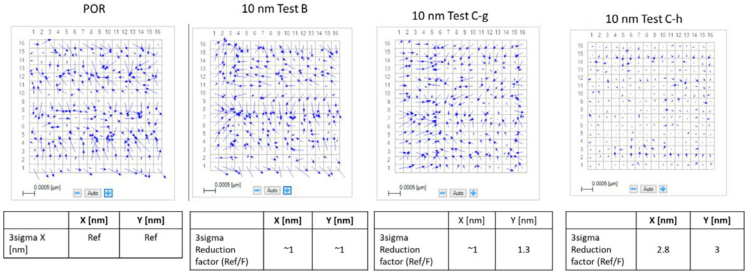


Figure 6. LER and LWR comparing the current performance POR and the two 10nm test cases B and C. (a) shows the results obtained using the pattern discussed in Figure 5 and (b) shows LER power spectrum results obtained using the LCDU pattern discussed in Figure 4. In addition to LCDU, LER and LWR were both improved by the use of the 10nm spot size.



	X [nm]	Y [nm]
3sigma X [nm]	Ref	Ref

	X [nm]	Y [nm]
3sigma Reduction factor (Ref/F)	~1	~1

	X [nm]	Y [nm]
3sigma Reduction factor (Ref/F)	~1	1.3

	X [nm]	Y [nm]
3sigma Reduction factor (Ref/F)	2.8	3

Figure 7. Local registration performance as a function of write modes. Test C-h shows the most improvement.

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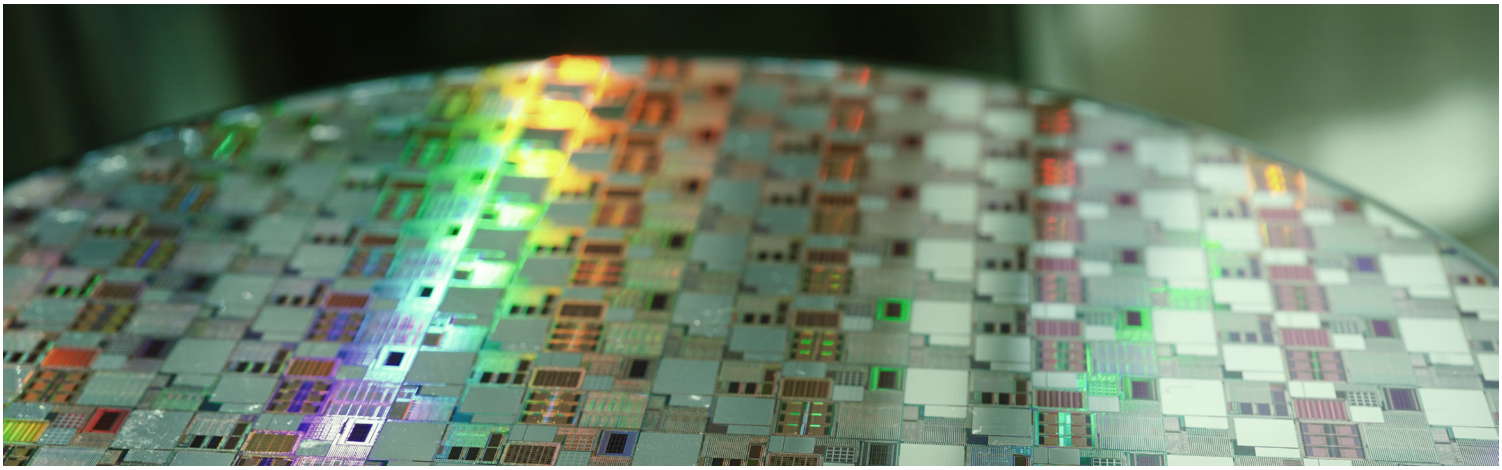

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INDUSTRY BRIEFS

“This is really bad,” says TSMC CEO, C.C. Wei

“Geopolitical confrontation has distorted the entire market,” Wei told a forum organized by the Monte Jade Science and Technology Association. “The situation has destroyed all the productivity and efficiency brought by globalization,” added Wei, “even if saying destroying is too strong, these barriers will seriously affect the benefits of a free economy like in the past. This is really bad.”

https://www.electronicsweekly.com/news/business/this-is-really-bad-says-tsmc-ceo-2022-12/

Rallying Cry from imec CEO Luc Van den hove

Imec CEO Luc Van den hove has called for a renewal of the spirit of international cooperation which has driven the semiconductor industry’s extraordinary progress and could be harnessed to solve the world’s political challenges.

https://www.electronicsweekly.com/news/business/rallying-cry-from-imec-ceo-2023-01/

Taiwan Passes its Chips Act, Offers Tax Credits to Chipmakers

Bloomberg

Taiwanese lawmakers have passed new rules that let local chip firms turn 25% of their annual research and development expenses into tax credits, part of efforts to keep cutting-edge semiconductor technologies at home and maintain the island’s technology leadership. “As the United States, Japan, South Korea and the European Union are all offering massive incentives to build domestic supply chains, Taiwan should bolster the global competitiveness of its key industries,” Taiwan’s Ministry of Economic Affairs said in a statement on Saturday.

https://www.moneyweb.co.za/news/tech/taiwan-passes-its-chips-act-offers-tax-credits-to-chipmakers/

Intel’s Mobileye Sees $17 Billion in Assisted-Driving Product Revenues by 2030

Reuters

Intel Corp’s self-driving tech unit Mobileye Global Inc. said on Thursday it sees more than $17 billion in revenues for its advanced driver assistance systems (ADAS) products by 2030.

https://money.usnews.com/investing/news/articles/2023-01-05/intels-mobileye-sees-17-billion-in-assisted-driving-product-revenues-by-2030

QoQ Decline in DRAM ASP Will Moderate to Around 13~18% for 1Q23

TrendForce’s latest analysis of the DRAM market finds that the inventory pressure on suppliers remains significant due to the persistently weak demand for consumer electronics.

https://evertiq.com/news/53105

Samsung’s Quarterly Profit Hits 8-Year Low Amid Weak Demand for Memory Chips, Smartphones

Samsung Electronics’ operating profit plummeted 69% to $3.4 billion in the quarter that ended in December to an eight-year low, according to its preliminary estimates, as the global demand for memory chips and smartphones wanes due to high inflation and a slowing economy.

https://techcrunch.com/2023/01/06/samsungs-quarterly-profit-hits-8-year-low-amid-weak-demand-for-memory-chips-smartphones/

$30m for Open Source End-to-End FPGA Software

Rapid Silicon is raising $30m to boost the rollout of its end-to-end open source FPGA software and entry level hardware.

https://www.eenewseurope.com/en/30m-for-open-source-end-to-end-fpga-software/

Future Transistors, Plastic Processors, and 3D Chips

IEEE Spectrum’s biggest semiconductor headlines of 2022.

https://spectrum.ieee.org/3d-chips-plastic-processors

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Key dates

2023

SPIE Advanced Lithography + Patterning
26 February–2 March 2023
San Jose, California, USA
www.spie.org/al

SPIE Photomask Technology and EUV Lithography
1–5 October 2023
Monterey, California, USA
www.spie.org/puv

European Mask and Lithography Conference (EMLC)
19–21 June 2023
Dresden, Germany
www.emlc-conference.com

Photomask Japan (PMJ)
25–27 April 2023
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www.photomask-japan.org

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