APRIL 2023
VOLUME 39, ISSUE 4

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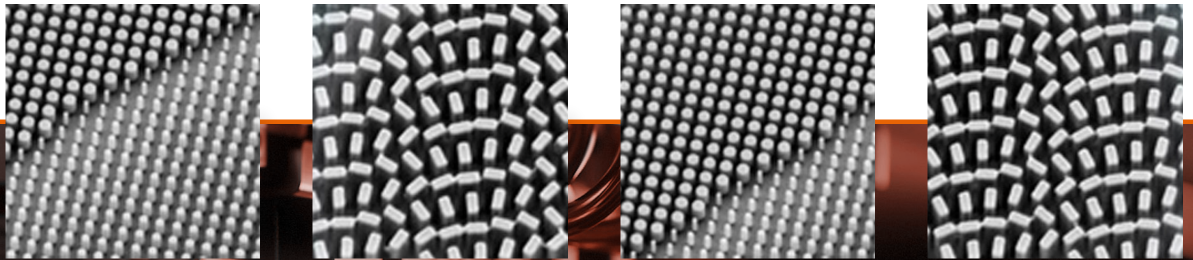
What is the value of a forecast?



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EDITORIAL

What is the value of a forecast?

Andy Wall, *HOYA Corporation*

Take yourself back to 2021. The world was wearing masks and sanitizing their hands. We were all working in a "temporary" space that we had set up at home more than a year earlier. The world wasn't a happy place, but the semiconductor industry thrived as demand for PCs, smartphones and digital communication continued to grow. Industry veterans understand the historically cyclical nature of the market, but in 2021 many of the commercial forecast services predicted a new normal, where semiconductor demand will continue to grow at a strong pace for years to come. Yet here we are in 2023 with declining consumer demand and an unexpected slowdown in the market. Employee lay-offs and cost-cutting are the new normal and so what value is a forecast?

Those of us in the industry with internal forecasting roles often recognized and discussed the possibility of a downturn coming, even while the public models continued to show ongoing growth. The extent to which this was built into internal company forecasts vary, and externally the forecast function often suffers from "groupthink" and aligns to a common public message which leads to the question of what value they provide, especially after an unanticipated shift in the industry.

Forecasts act as a reference and are a starting point for market knowledge that can be criticized, debated and adapted by both the internal company teams and externally at industry forums, including conferences and workshops. Any forecast holds a value, but first it is important to understand that being wrong is the natural state of a forecast! The world is littered with examples of bad forecasts; In 1959 IBM thought that the world potential market for copying machines was 5,000, at most, but within a couple of years the Xerox 914 copier machine became one of the most successful products of all time. Microsoft CEO Steve Ballmer said in 2007 that the iPhone doesn't appeal to business customers because it doesn't have a keyboard, and the rest is history. For a forecast to hold value, you need to know how to read it. A forecast is an opinion. A forecast number or statement acts only as a reference, and it is the discussion, understanding, and debate about the assumptions behind the forecast that is of value and leads to a greater understanding of the industry in which we work. They continue to hold value, even if they are wrong.

So, if all forecasts are wrong, can we predict when the industry recovers? The industry is generally aligned to recover in the second half of 2023, which is a vague timeline, and remember the influence of groupthink on these forecasts. If we look at the semiconductor industry today, we see record inventory, declining ASPs, and consumer demand continue to slow. The indicator trends are on a continuing trajectory and have not started to reverse. The conditions in the market suggest that a recovery at the beginning of the second half of the year, which is just two months away, may be optimistic, but you should use the forecast as intended, which is an opinion and one view of the future. Discuss, debate, and criticize, and together we can build a stronger view of the future, but we will always be wrong. The question is how wrong will we be?

The opinions expressed in this editorial are personal and do not constitute those of the company the author is working for.

BACUS News is published monthly by SPIE for BACUS, the international technical group of SPIE dedicated to the advancement of photomask technology.

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FEATURED ARTICLE

Nanoimprint Performance Improvements for High-Volume Semiconductor Device Manufacturing

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Abstract

Imprint lithography is an effective and well-known technique for the replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, the resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single-level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

Memory fabrication is challenging, in particular for DRAM, because the roadmap for DRAM calls for continued scaling, eventually reaching half pitches of 14nm and beyond. For DRAM, overlay on some critical layers is much tighter than NAND Flash, with an error budget of 15-20% of the minimum half pitch. For 14nm, this means 2.1-2.8nm. DRAM device design is also challenging, and layouts are not always conducive to pitch-dividing methods such as SADP and SAQP. This makes a direct printing process, such as NIL an attractive solution. Logic is more challenging from a defectivity perspective, often requiring defect levels significantly lower than memory devices that incorporate redundancy.

In this paper, we touch on the markets that can be addressed with NIL and describe the efforts to further improve NIL performance. We specifically focus on performance improvements related to overlay and defectivity. For overlay, we present results on stability and discuss new methods to further address high-order distortion. For defectivity, we review random defect generation, particle adders, and mask inspection methods. In addition, we also discuss Canon's recent involvement in the New Energy and Industrial Technology Development Organization (NEDO) project and its goals related to logic devices. As a final topic, we describe Canon's interests in fabrication beyond traditional advanced semiconductor devices.

Introduction

Imprint lithography is an effective and well-known technique for the replication of nano-scale features.[1,2] Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.[3-9] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, the resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single-level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

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Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay, and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In 2018, Hiura et al. reported a mix-and-match overlay (MMO) of 3.4 nm and a single-machine overlay (SMO) across the wafer was 2.5nm using an FPA-1200 NZ2C four-station cluster tool.[10] These results were achieved by combining a magnification actuator system with a High Order Distortion Correction (HODC) system, thereby enabling the correction of high-order distortion terms up to K30.

In this paper, we touch on the markets that can be addressed with NIL and also describe the efforts to further improve NIL performance. We specifically focus on performance improvements related to overlay and defectivity. For overlay, we present results on stability and also discuss new methods to further address high-order distortion. For defectivity, we review random defect generation, particle adders, and mask inspection methods. In addition, we also discuss Canon's recent involvement in the New Energy and Industrial Technology Development Organization (NEDO) project and its goals related to logic devices. As a final topic, we describe Canon's interests in fabrication beyond traditional advanced semiconductor devices.

NIL Applications and Markets

Unlike other patterning methods for semiconductor devices, NIL has the potential to impact additional markets, as illustrated in Figure 1. Beyond, memory and logic, the device space covered includes CMOS image sensors, diffractive optical elements, and meta-optical elements (MOEs). In this paper, we discuss memory fabrication status, logic, and MOEs. For the memory topic, we specifically address performance improvements related to overlay and defectivity.

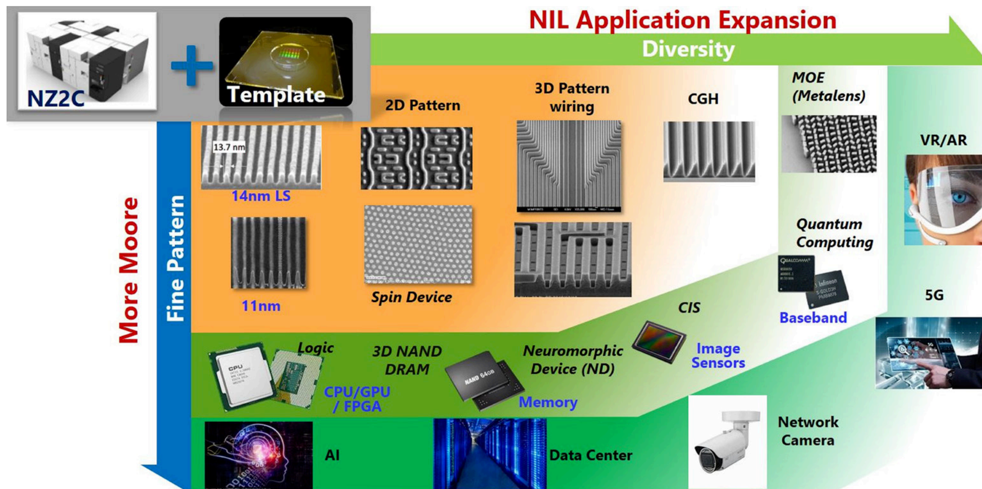

Figure 1. Potential application space for NIL.

		2022-2024	2025-2027	2028 →	NIL Status
3D NAND					- Patterning and overlay are satisfied - Productivity will determine the insertion point for MP
	L/S (min hp)	~20nm	~20nm	~20nm	
	Overlay	5nm	5nm	5nm	
DRAM					- Patterning good down to 14nm - Overlay needs to be demonstrated
	L/S (min hp)	14-12nm	11-10nm	≤10nm	
	Overlay	2.8-2.4nm	2.2-2.0nm	≤2.0nm	
Logic					- Patterning requires improvements in template technology starting at 3nm - Defectivity is still challenging
	L/S (min hp)	12nm	10nm	8nm	
	Overlay	2.4nm	2.0nm	1.6nm	
Mask Roadmap*					
	14nm hp L/S	Production			
	10nm hp L/S		Production		
	8nm hp L/S			Production	

Figure 2. NIL Roadmap for advanced semiconductor devices.

Overlay

Recent efforts have focused on the development of NIL for advanced memory applications such as 3D NAND Flash and DRAM. DRAM memory is challenging, because the roadmap for DRAM calls for continued scaling, eventually reaching half pitches of 14nm and beyond. For DRAM, overlay on some critical layers is much tighter than NAND Flash, with an error budget of 15-20% of the minimum half pitch. For 14nm, this means 2.1-2.8nm. A device roadmap, which includes DRAM overlay requirements is shown in Figure 2. DRAM device design is also challenging, and layouts are not always conducive to pitch-dividing methods such as SADP and SAQP. This makes a direct printing process, such as NIL an attractive solution.

To address overlay in a Nanoimprint system, there are many factors that need to be considered, some of which are quite different than what is required for photolithographic tools. In optical lithography, High Order Compensation is done by manipulating both the lens and stage during the exposure process. A different approach is required for nanoimprint. High Order Distortion Correction (HODC) for NIL can be enabled by combining two techniques.

- One is using Magnification actuators, which apply force using an array of piezo actuators.
- And the second is Heat input, which is supplied by a DMD to correct distortion on a field-by-field basis.

The HODC method has been presented in the past, and recently additional corrections methods have been applied in order to drive cross-matched machine overlay (XMMO) to an ArF immersion scanner down to 2nm. Additional terms include:

- Drop Pattern Compensation
- Imprint Force
- Imprint tip/tilt control
- Refined mask
- Wafer zone chuck pneumatics

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Details on these correction methods can be found in references 11-13. Figure 3 schematically illustrates the various tuning knobs used for NIL.

For the case of 3D NAND Flash, overlay targets are typically less than 5nm, and recent efforts have focused on overlay stability. Presented in Figure 4 is a graph of overlay in x and y as a function of time, covering a 3.5-month span. Results are consistently under 4nm and in many cases less than 3nm.

For DRAM fabrication, the target is 2nm and it, therefore, becomes necessary to incorporate other techniques to reduce the overlay error. Past papers have discussed the use of a "refined" mask, in which distortion errors are fed back to a second mask to better match the original ArF immersion field. Partial fields (PF) are particularly challenging, and a new method referred to as a control point for alignment, or point of interest, has been applied. With this method, the control point for alignment is placed relative to the center of the through-the-mask (TTM) marks, thereby accelerating alignment convergence and reducing overlay errors in the partial fields.[14] The method is illustrated in Figure 5.

In Figure 6, we compare the best XMMO results from 2021 and 2022. In both cases, NIL was matched to an ArF immersion scanner, and the reported results show the measurements for all fields, 322 locations per field. The

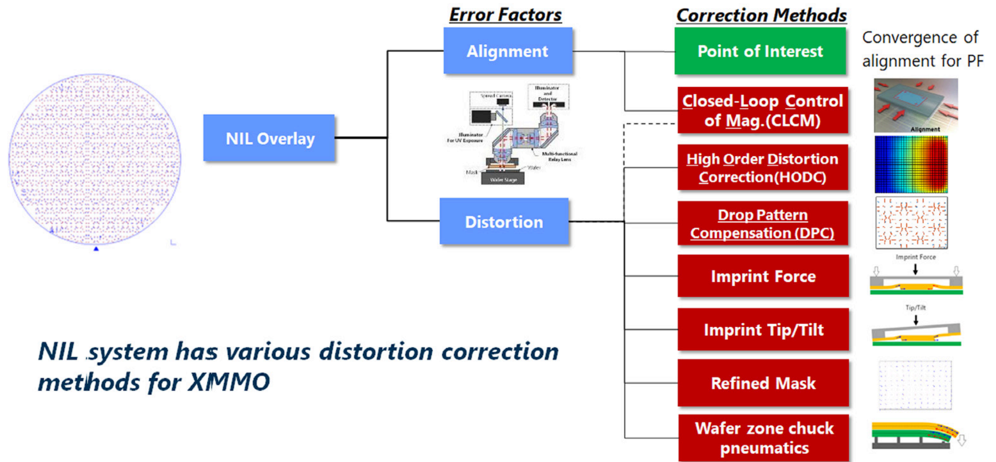

Figure 3. To address overlay, there are many factors that need to be considered. Generally speaking, the process can be broken down into two categories: Alignment and Distortion.

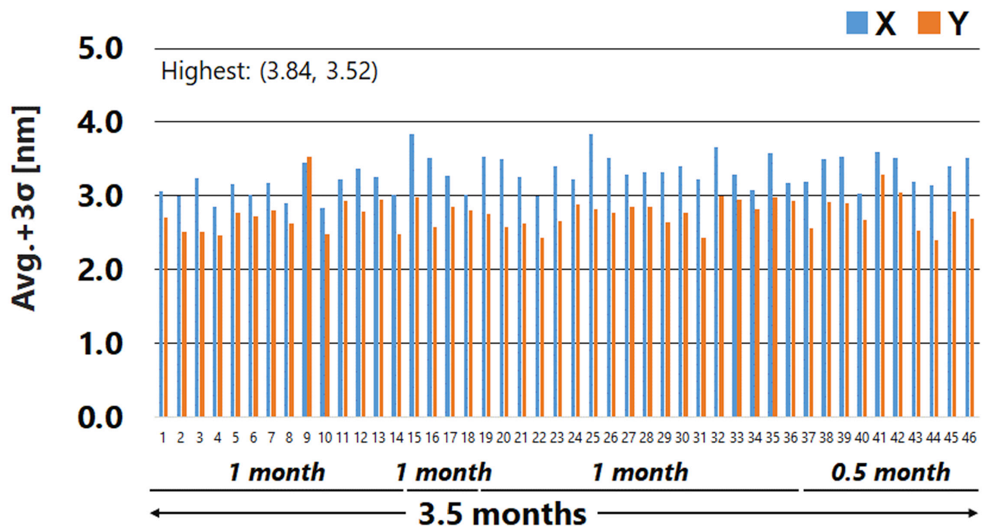

Figure 4. Overlay stability covering 3.5 months.

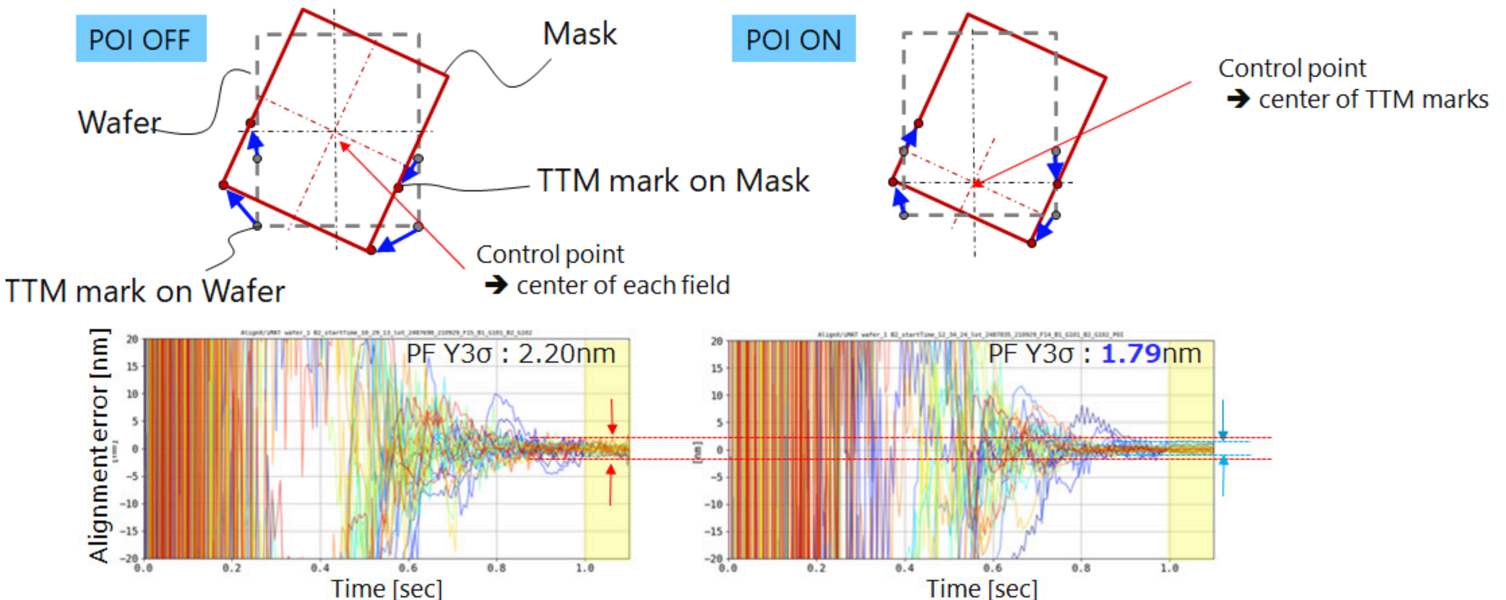

Figure 5. Effect of the control point for alignment (POI).

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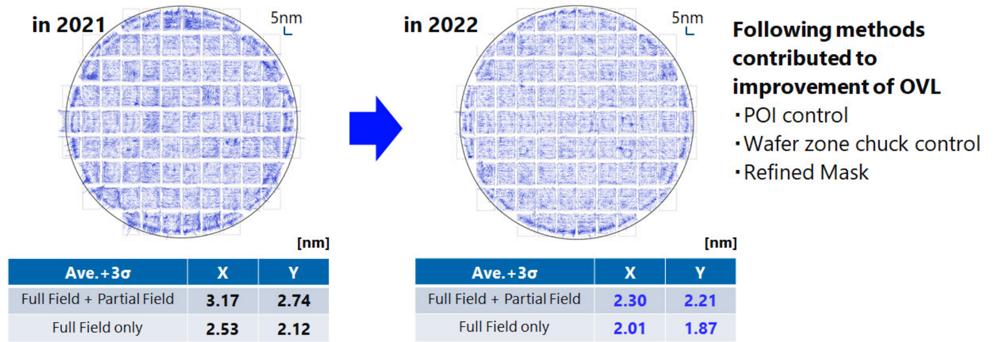
improvement in 2022 is obvious. Full-field XMMO was on the order of the 2nm mean plus three sigma. Full fields and partial fields results were slightly higher, with x and y values of 2.30nm and 2.21nm, respectively.



Ave.+3σ (2021)	X	Y
Full Field + Partial Field	3.17	2.74
Full Field only	2.53	2.12

Ave.+3σ (2022)	X	Y
Full Field + Partial Field	2.30	2.21
Full Field only	2.01	1.87

Figure 6. Full-field and partial-field NIL cross-matched machine overlay.

Defectivity

Defectivity, even for the memory market, plays a critical role and it is important to minimize random occurring defects, avoid particle formation that creates permanent defects in the mask, and carefully inspect the imprint mask to keep track of defects that are formed and better characterize mask lifetime.

In the case of random defectivity, the predominant defects are non-fill and feature collapse. In Figure 7 we plot random defectivity as a function of time for a period of 3.5 months. The data set includes measurements from 25 wafers covering, a three-month time span. Defectivity was measured using a KLA 2905 system. Repeating defects were extracted using Klarity software, and defect types were confirmed by SEM review. In all cases, random defectivity was less than 0.03 defects/cm^2, and for several cases was well under 0.01 defects/cm^2.

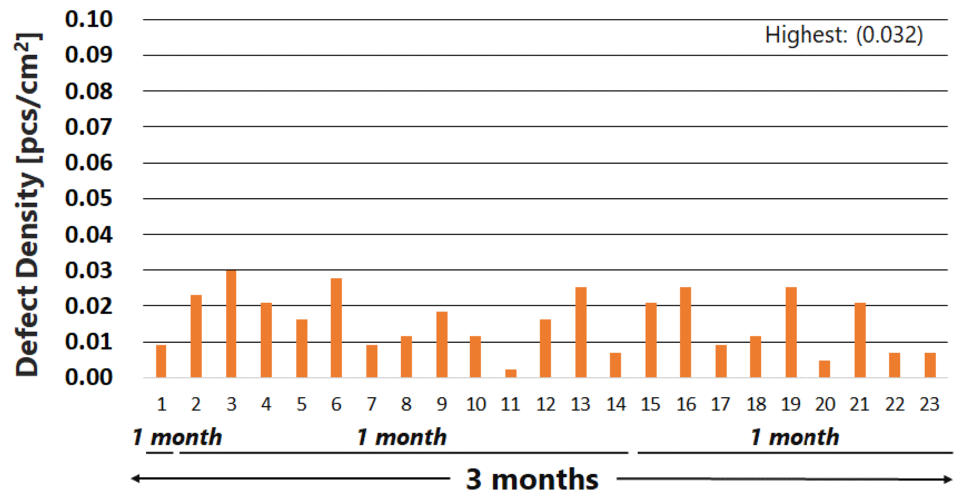


Figure 7. Random defectivity as a function of time. Defectivity is less than 0.03 defects/cm2, and for several cases is well under 0.01 defects/cm2.

Permanent or repeater defects are typically caused by hard particles introduced either by the tool or incoming wafers. In the past, several papers have discussed methods for suppressing particle generation.[15] In this paper, we review particle adders as a function of time across six different imprint stations. For a mask lifetime of 80 lots or two thousand wafers which meets a defect spec of 0.02 defects/cm^2, the particle adder target is one defect every 10,000 wafers. This is now being achieved in multiple stations.

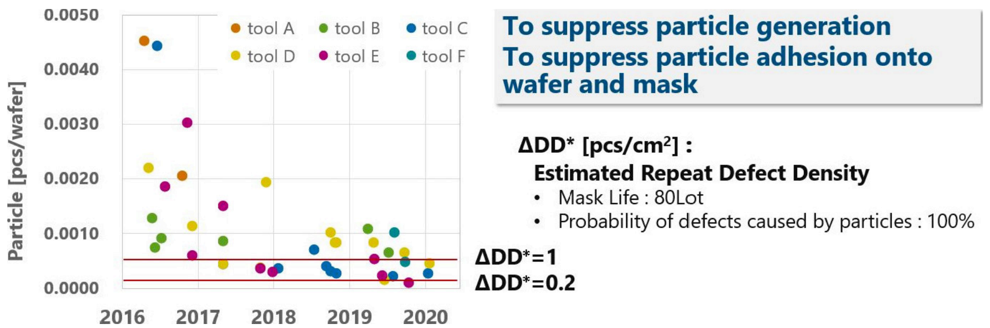


Figure 8. Particle adder counts for multiple imprint stations.

To further suppress particle adders and minimize defectivity, new methods are being studied and are planned for future implementation on NIL tools. Offline cleaning of masks is already implemented, and the next steps include in-situ mask cleaning and wafer particle inspection, as illustrated in Figure 9. The wafer particle checker (WPC) is already under development and its performance on bare wafers has been compared to a KLA SP3 particle inspection tool (Figure 10). Wafers were prepared with an array of calibrated spheres and the data confirms that the resolution of the WPC is 200nm. WPC inspection time is approximately 13 seconds per wafer. The next steps include characterizing the WPC on patterned wafers and installing it on an NZ2C system.

Logic

A second market of interest is logic, and in 2021 Canon applied to the New Energy and Industrial Technology Development Organization (NEDO) for a grant project on extended miniaturization for logic devices along with other key semiconductor manufacturing equipment companies in Japan. The program was approved, and the subject

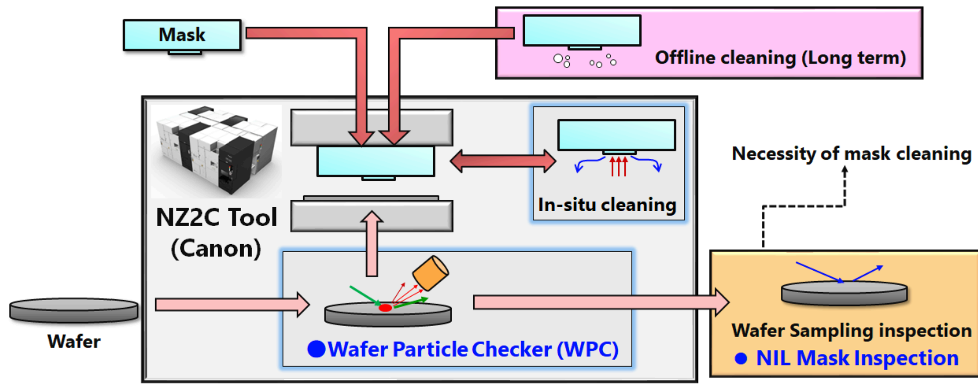


Figure 9. Mask management. To further suppress particle adders and minimize defectivity, new methods are being studied and are planned for future implementation on NIL tools.

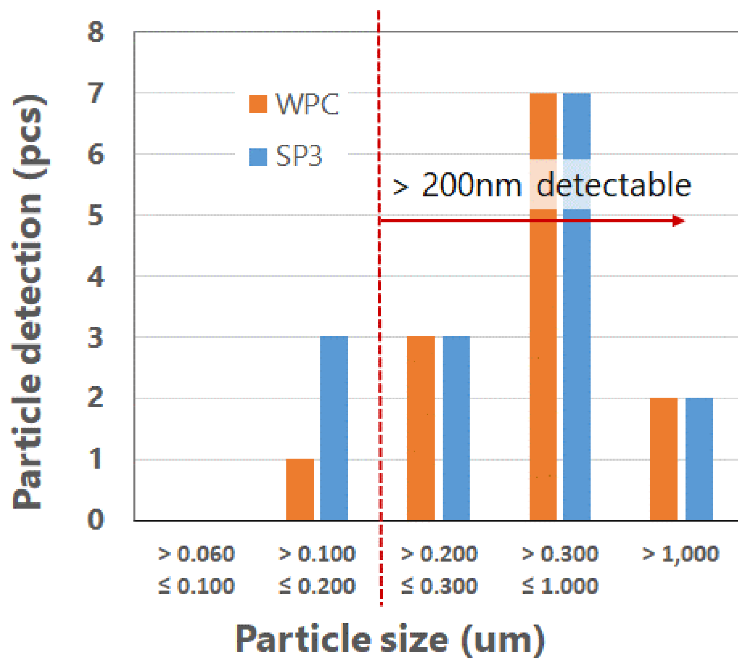


Figure 10. Resolution comparison between a KLA SP3 and the WPC.

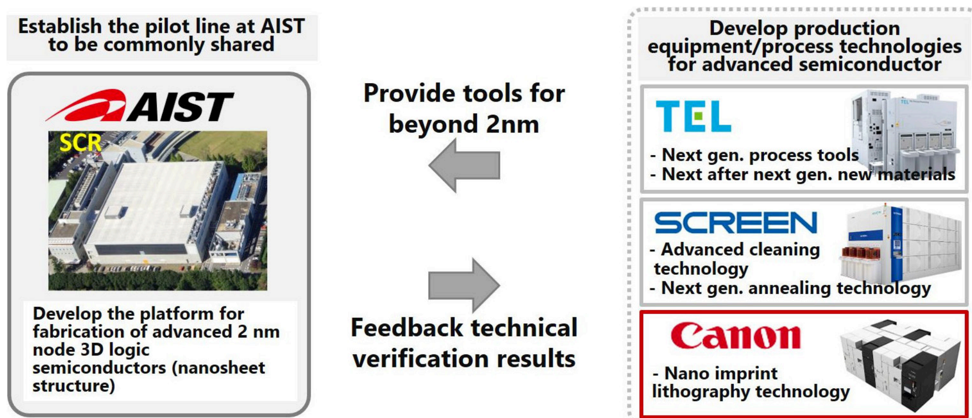


Figure 11. Schematic of the NEDO manufacturing development program.

matter is the extension of logic-based devices after the 2nm node. Included in the program is the implementation and verification of nanofabricated wafers using a shared pilot line at the National Institute of Advanced Industrial Science and Technology (AIST). A schematic illustration of the NEDO project organization is shown in Figure 11.

Development work will target nanosheet devices as shown in the figure below. In this program, Canon will develop NIL technology for the patterns of 12nm half pitches and below, in collaboration with AIST which evaluates the pattern practicability in the device integration.

Also being considered is the application of NIL for dual damascene structures that are common in the back end of line layers.[16] Motivation is the reduction of cost of ownership using a NIL process that can define both the line and via, as illustrated in Figure 13.

Meta Optical Elements (MOEs)

Meta optical elements or MOEs are a type of patterned metasurface.[19,20] A potential use for these devices is optical elements that are used in cameras, mobile phones, and other devices that typically rely on shaped lenses that focus light to form an image. With the introduction of metasurfaces, it becomes possible to shrink lenses and remove constraints of the past. Metasurfaces typically refer to the two-dimensional counterparts of metamaterials. Metasurfaces can be either structured or unstructured with subwavelength-scaled patterns in the horizontal dimensions.

Because metalenses are flat (planar) and ultra-thin, they do produce chromatic aberrations—they are “achromatic”—because all wavelengths of light pass through virtually simultaneously. Their advantages also include tunable dispersion—the ability to manipulate how colors of light are dispersed—as opposed to glass or other traditional materials that have fixed dispersions. Wavelengths of interest cover both infrared and the UV/Vis spectrum.

In the examples shown in the figure to the right, note the changes in feature size and direction of the elements. Early work on MOEs mainly relied on electron

beam writing, which is appealing for prototyping, but not for production. NIL is an appealing choice for the production patterning of MOEs because of the few patterning constraints associated with the technology.

Conclusions

Imprint lithography is an effective and well-known technique for the replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, the resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single-level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

In this paper, we have touched on the markets that can be addressed with NIL, including advanced memory, logic, and meta-optical elements. We also described the efforts to further improve NIL performance, covering both overlay and defect mitigation. On the topic of overlay, both stability and distortion methods were discussed. Full-field XMMO was on the order of the 2nm mean plus three sigmas. Particle adders have been reduced to about one per every 10,000 wafers. Also introduced was the New Energy and Industrial Technology Development Organization (NEDO) project on extended miniaturization for logic devices along with other key semiconductor manufacturing equipment companies in Japan. The program is focused on extending logic beyond the 2nm node.

As a final topic, we discussed Canon's interests in patterning metalenses which have the potential to shrink lenses and remove current design constraints.

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YEAR OF PRODUCTION	2020	2022	2025	2028	2031
Logic industry "Node Range" Labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"
Device structure	2.5D-structure		3D-structure		
Mainstream device for logic	finFET	finFET	Nanosheet LGAA	Nanosheet LGAA	LGAA-3D-stack
Beyond-CMOS as complimentary to mainstream CMOS	-	-	-	2D Device, FeFET	2D Device, FeFET
Channel material technology inflection	SiGe25%	SiGe50%	SiGe50%	Ge, 2D Material	Ge, 2D Material
LOGIC DEVICE GROUND RULES					
Lg: Gate Length - HD (nm)	20	18	14	12	12
M0 half-pitch: hp (nm)* = "Pitch / 2"	15	12	10	8	8

Figure 12. Development target of nanosheet devices.

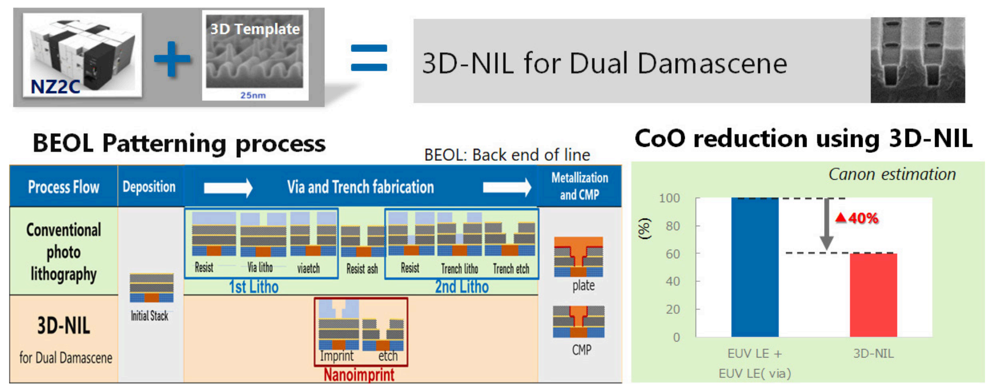

Figure 13. Back end of line processing. NIL has the potential to significantly reduce the cost of ownership.

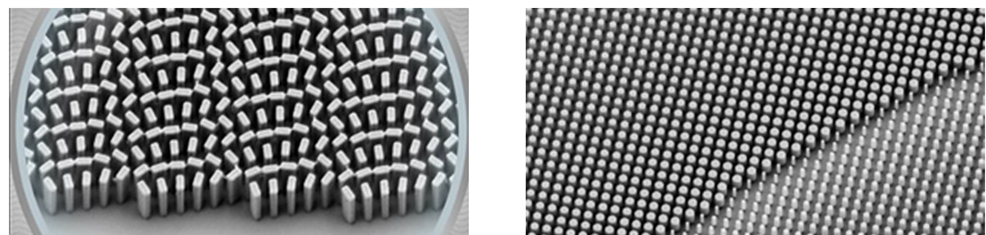

Figure 14. Examples of meta-optical elements. MOE patterns can be configured to operate either in the infrared or UV/V spectrum.

Acknowledgments

The authors gratefully acknowledge their coworkers at Canon Inc. and Canon Nanotechnologies Inc. for their support of this work.

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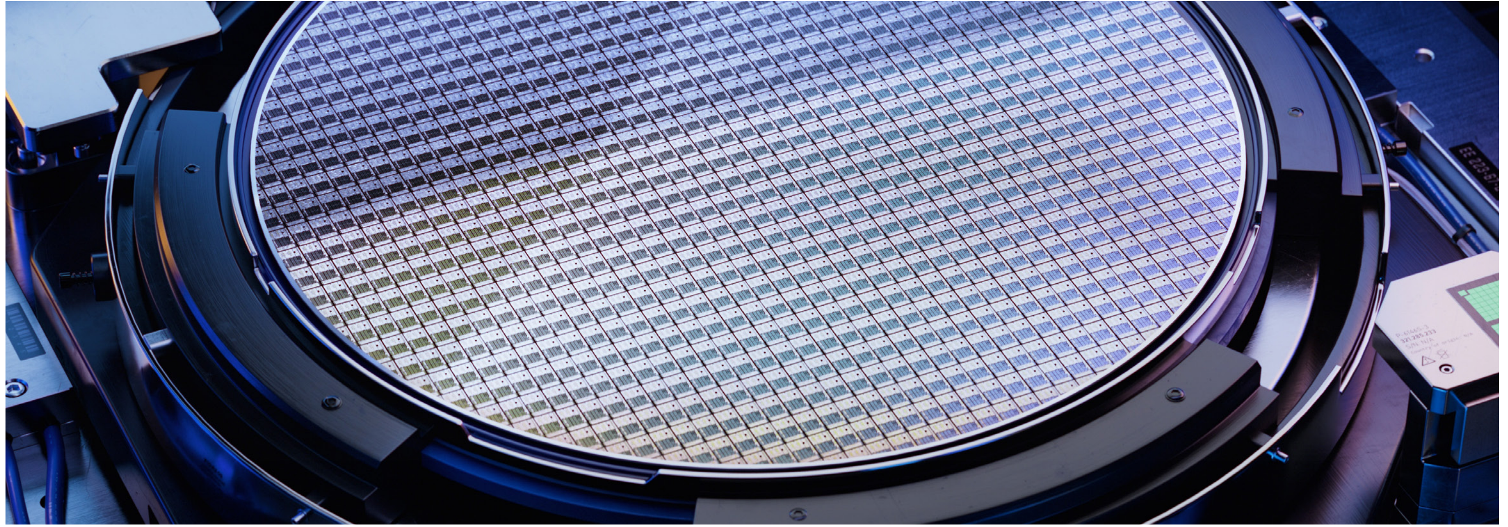

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INDUSTRY BRIEFS

NVIDIA speeds key chipmaking computation by 40x with GPUs

Through the use of GPUs, NVIDIA has demonstrated that Inverse-lithography can be sped up to the point of being viable for full chip manufacture. Inverse lithography's use has been limited by the massive size of the needed computation. Nvidia's answer, cuLitho, is a set of algorithms designed for use with GPUs, turns what has been two weeks of work into an overnight job.

spectrum.ieee.org/inverse-lithography

Large-scale nanometer-thick graphite film (NGF) as a EUV pellicle (3/18)

To address defect protection, options for EUV pellicle materials continue to be explored. A nanometer-thick graphite (NGF) has demonstrated tremendous potential for addressing optical, mechanical, thermal, and chemical criteria among potential pellicle materials such as carbon allotropes, Si, SiNx, and Si-Mo-Nb.

semiengineering.com/large-scale-nanometer-thick-graphite-film-ngf-as-a-euv-pellicle/

EUV tech and IBM join the ebeam initiative (2/28)

The eBeam Initiative, a forum dedicated to the education and promotion of new semiconductor manufacturing approaches based on electron beam (eBeam) technologies, announced the addition of two new company members to the organization: EUV Tech, a pioneering leader in actinic EUV metrology equipment; and IBM, an industry leader and pioneer in advanced patterning technology

www.eejournal.com/industry_news/euv-tech-and-ibm-join-the-ebeam-initiative/

Government of Canada invests in Ranovus to further advance Canada's semiconductor industry (3/27)

To support the expansion of one of Canada's homegrown semiconductor companies, Minister of Innovation, Science and Industry, announced a $36 million contribution through the Strategic Innovation Fund (SIF) to Ottawa-based Ranovus Inc. to support a $100 million project that will advance the domestic production and manufacturing of semiconductor products and services, while positioning Canada as a key player in this strategic industry.

finance.yahoo.com/news/government-canada-invests-ranovus-further-153900557.html?guccounter=1

Taiwan, Czech Republic to deepen semiconductor cooperation (3/28)

Extending on historical collaboration in science and technology, Taiwan will share its semiconductor experience and know how to enhance the Czech Republic's chip design research. The National Science and Technology Council (NSCT) has signed agreements with the Technology Agency of the Czech Republic, Czech Science Foundation, Czech Science Foundation, and the Czech Academy of Sciences, he said, adding that Taiwan and the Czech Republic continue to jointly subsidize cooperative research and personnel exchange programs every year.

www.taiwannews.com.tw/en/news/4848629

First CHIPS for America funding opportunity launched (2/28)

The Biden-Harris Administration through the U.S. Department of Commerce's National Institute of Standards and Technology today launched the first CHIPS for America funding opportunity for manufacturing incentives to restore U.S. leadership in semiconductor manufacturing, support good-paying jobs across the semiconductor supply chain, and advance U.S. economic and national security.

www.commerce.gov/news/press-releases/2023/02/biden-harris-administration-launches-first-chips-america-funding

ASML, China customers haunted by uncertainty on new Dutch chip export rules (3/9)

New rules by the Dutch government set to potentially limit export of key semiconductor lithography equipment by ASML Holding NV to China customers.

www.reuters.com/technology/asml-china-customers-haunted-by-uncertainty-new-dutch-chip-export-rules-2023-03-09/

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spie.org/bacushome

Key Dates

2023

SPIE Photomask Technology and EUV Lithography
1–5 October 2023
Monterey, California, USA
www.spie.org/puv

European Mask and Lithography Conference (EMLC)
19–21 June 2023
Dresden, Germany
www.emlc-conference.com

Photomask Japan (PMJ)
25–27 April 2023
Online only
www.photomask-japan.org

2024

SPIE Advanced Lithography + Patterning
25–29 February 2024
San Jose, California, USA
www.spie.org/al

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