**Lab – D FLIP-FLOPS**

**Objectives:**

- Investigate the operation of a D flip-flop

- Investigate what the various pins of the flip-flop do

-Observe the output of a flip-flop for a given input and draw timing diagrams

**Equipment:**

One IC 7474 Dual D-type flip-flops, two 1k Ohm and two 330 ohm resistors, One DIP switch, and one push button switch (N.C. or N.O.)

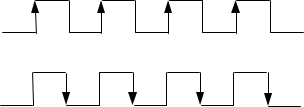
IC Pin Diagrams

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# Introduction:

A flip-flop is a binary storage device capable of storing one bit of information. It is a basic building block for counters, registers, and other sequential control logic.A flip-flop circuit can maintain a binary state indefinitely until directed by an input signal to switch state.

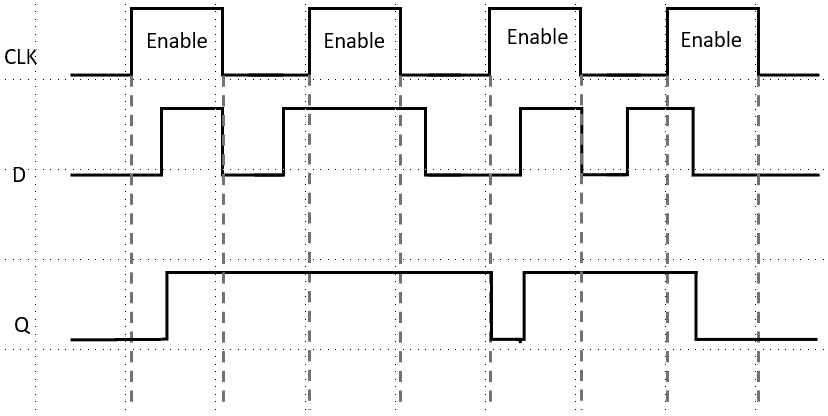
Flip-flop circuits are constructed in such a way as to make them operate properly when they are part of a circuit that employs a steady oscillating signal called a ‘clock’. A flip-flop uses an edge detection circuit to trigger it only during a clock signal transition. A clock pulse goes through two transitions from 0 to 1 (positive-edge transition) and from 1 to 0 (negative-edge transition) as shown in Figure 1.



*Figure 1*. – A Clock Pulse

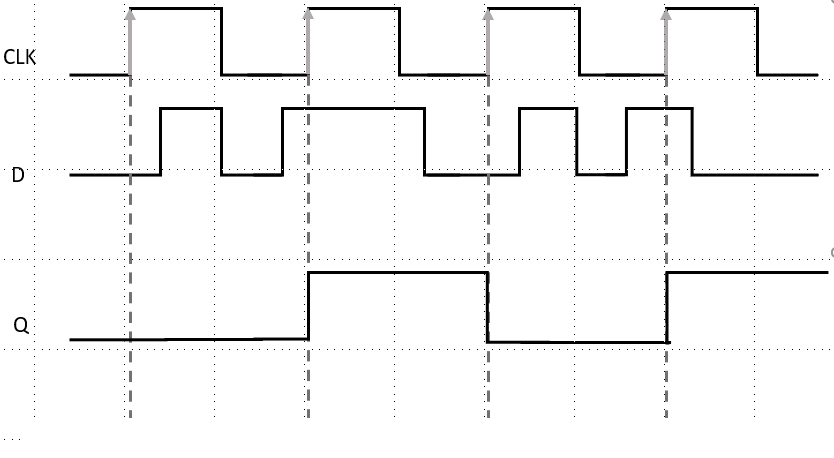
In last week’s lab, you saw that a D latch is used to capture, or 'latch' the logic level which is present on the Data line when the Enable (also known as the Clock) input is high. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input, D. When the CLK input falls to logic 0, the last state of the D input is trapped and held in the latch. The action of a D-Latch is summarized in the timing diagram below. You can see the output Q follows the D input only when the CLK level is high. When the CLK level is low, the output of Q is the same as the last state of D the instant before the CLK level transitioned to a low state.

**Timing diagram of a D-Latch**

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*Figure 2 - Timing diagram of a D-Latch*

 A D flip flop is similar to the D latch except that the output of D Flip Flop takes the state of the D input at the moment of a positive edge transition at the clock pin (or negative edge transition if the clock input is active low).

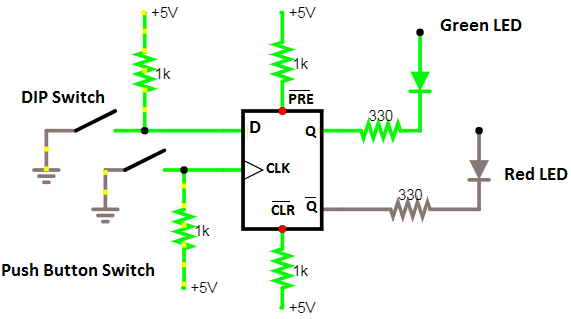


*Figure 3 - Timing diagram of a D-Flip Flop*

From the timing diagram it is clear that the output Q changes only at the positive edge transition of the clock signal indicated by the up arrows. At each positive signal edge, the output Q becomes equal to the input D at that instant and this value of Q is held until the next positive edge.

# Procedure

1. Connect one D-flip flop from the IC 7474 as follows:
   1. Connect input D to a DIP switch.
   2. Connect PRESET(PRE) and CLEAR(CLR)inputs to two 1k Ohm resistors connected to 5V
   3. Connect CLK input to a push-button switch
   4. Connect outputs Q and Q’ to a green and red LED, respectively.



*Figure 4* – D Flip-Flop Circuit[[1]](#endnote-1)

1. After wiring the circuit in figure 2, turn on the power to the breadboard and note the initial state of output Q. In this circuit, the red LED is on when Q = 1 and off when Q = 0.

3.Set the DIP switch (i.e. – top switch) so that the input of D is a low and observe what happens to the output Q.

4.Now press the push button switch (lower switch) once and observe the state of Q.

**Question1:** What happens to the output Q when the push-button switch was pressed?

**Question2:** What happens to output Q if you press the switch a number of times?

5. Set the DIP switch so that the input of D is high and observe what happens to the output Q.

6.Now press the push button switch once and observe.

**Question3:** What happens to the output Q?

7. Set the CLR input of the flip flop to a low (ground) and repeat steps 3-6 above.

**Question4:** What happened to the state of Q in each case?

8. Set the CLR input back to a high and set the PRE input of the flip flop to a low (ground) and repeat steps 3-6 above. Observe the state of Q in each case.

**Question5:** What happened to the state of Q in each case?

**Data and Observations**

Summarize your observations above in the logic table below. Record the logic states.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLK** | **D** | **CLR** | **PRE** | **Q** |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

**Mini-Project**

**A picture containing clock

Description automatically generated**1.Wire up the IC 7474 flip-flop as shown below.

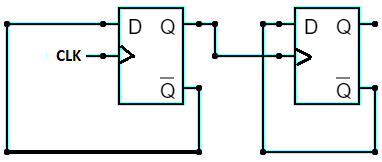
*Figure 5* – D Flip-Flop Circuit Modififed

2.Connect a wire from to the D input. Connect the frequency generator to the CLK input. Use a 5V square wave with a frequency of 100 Hz**.**

3**.**Use the Channel 1 of the oscilloscope to measure the input signal at the CLK and use Channel 2 of the oscilloscope to measure output at Q. **Note:** You might need to trigger the scope using the channel that has the slowest waveform.

4.Sketch a timing diagram for both CLK and Q below.

**Question6:** In what way has the signal at the output Q changed compared with that of CLK? *Hint:* Look at the period and frequency of the signal.

****5.Wire up the circuit below using two IC 7474 flip-flops.

*Figure 6* – Two D Flip-Flop Circuit

6**.**Use Channel 2 of the oscilloscope to measure output at Q which is output of the flip-flop furthest to the right in the diagram. Note: You might need to trigger the scope using the channel that has the slowest waveform.

7.Sketch a timing diagram for both CLK and Q

**Question7:** In what way has the signal at the output Q changed compared with that of the first circuit?

1. All schematic diagrams were created with Falstad circuit simulator (https://falstad.com/circuit/) [↑](#endnote-ref-1)