**Lab– Latches**

**Objectives:**

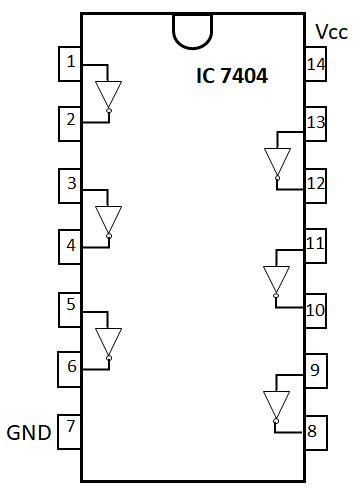
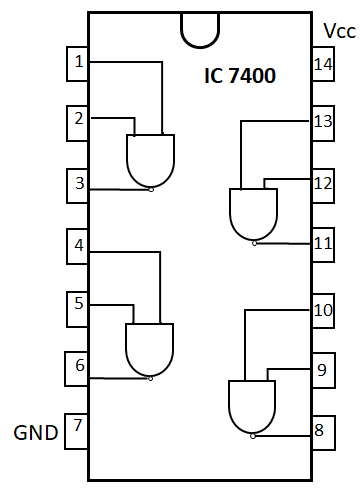
-To build an S-R Latch and determine its truth table

-Construct a gated D-Latch from NAND gates and an inverter and be able to explain its advantages compared to an S-R Latch

-To describe the main use of a latch and some of its applications

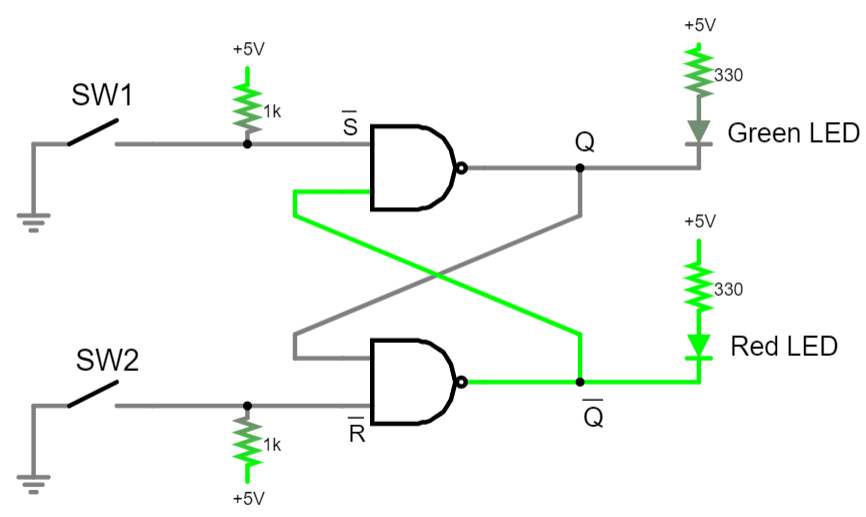
**Equipment:**

One Quad 7400 NAND gate; One 7404 Hex Inverter; Two 330 Ohm resistors; Two 1kOhm resistors; 1 Red LED; 1 Green LED; Two 2-pin push button switches (breadboard friendly); Function Generator.

IC Pin Diagrams

**Activity 1 – S-R Latch**

Build the following circuit on the breadboard. Note that unlike some of the circuits you’ve built in the previous labs, the LED is on when the output at Q (or ) is zero. In other words, when the output Q is zero then the green LED comes on when the output is zero the red LED comes on and thus Q=1.



*Figure 1- S-R Latch Circuit[[1]](#endnote-1)*

Examine the inputs ( & ) and outputs (Q & )of the circuit in figure1. Determine the truth table for this circuit. To make the input zero you just press the push button switch (SW1) and hold. To make input zero you just press the push button switch (SW2) and hold.

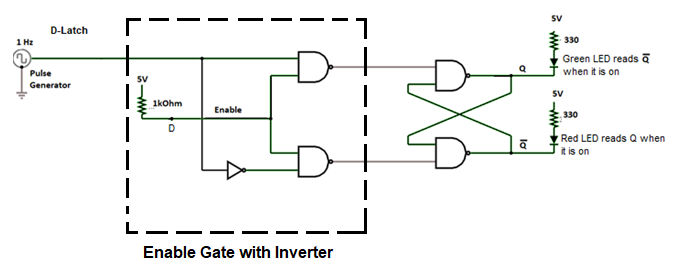
|  |  |  |  |
| --- | --- | --- | --- |
|  |  | Q |  |
| 0 | 1 |  |  |
| 1 | 0 |  |  |
| 1 | 1 |  |  |
| 0 | 0 |  |  |

**Question1:** Make the input of the NAND gate ‘0’ by pressing SW1 and holding. If push button SW2 is not pressed then the input should be one. What is the logic state of Q? What happens to the logic state at Q when you make the input of the NAND gate ‘1’ - did it change?

**Question2:** Now make the input of the NAND gate ‘1’ and the input ‘0’ by pressing and holding SW2. What is the logic state of Q? What happens to the logic state at Q when you make the input of the NAND gate ‘1’ again -did it change?

**Activity 2**

Whenever the set and reset inputs of an S-R Latch are both LOW, an invalid state results. A solution to this problem is to connect an inverter to the S-R Latch in such a way that the inputs to S and R can be better controlled. One way to accomplish this is with a D-Latch. A D-Latch uses an enable gate and an inverter to control whether both and can be LOW simultaneously. The enable gate with inverter circuit is shown in the figure below. When enable on the gate is set to HIGH, the inputs to the latch cannot be LOW simultaneously.

1.Use the pin diagrams above and wire up the circuit below. You will be building a D-Latch

*Figure 2- S-R Latch Circuit with an enable gate and inverter*

2.Make sure that you know which pins of the IC are the inputs and which are the outputs. Also, be sure you are applying power (Vcc) and ground to the correct pins of each IC otherwise your circuit will not function. The value of Vcc should be 5 Volts.

3. Connect the D input of the D-latch circuit to the TTL output of the function generator. Set the frequency to 5 Hertz. Connect the ‘Enable’ input to a HIGH through 1kOhm resistor (as shown in the circuit) and observe the output (Q). Now change the ‘Enable’ input to a LOW by connecting point D in the schematic to ground and observe the output.

4. Leave Enable LOW and place jumper wire from output Q to ground and then from output to ground.

**Data and Observations**

What are some of your observations for the D-Latch? Describe below. What does a latch do? Pay particular attention to how the state of the output (Q) compares with the state of the input (D) when the enable gate is set to HIGH or LOW.

1. All schematic diagrams were created with Falstad circuit simulator (https://falstad.com/circuit/) [↑](#endnote-ref-1)